Microstrip Patch Array Design

Antenna arrays offer improved directivity compared to a single-radiator antenna. The directivity of an array is due to interference effects between the individual elements of the array, which means that the spatial distribution of the elements as well as phases and magnitudes at each element need to be tuned for optimal performance.

Both the radiation pattern and S-parameters of the array is decided by several factors: the design of the individual patch element, the arrangement and spacing of the array, and the layout of the feed network. Each of these can be considered separately by dividing the process of designing the array into separate stages. By creating the array in steps, the task of optimizing the design is made less challenging, and the most appropriate tools can be used at each stage.

One common application of printed arrays is in wireless local area networks (WLAN). This article explains the design process for a planar microstrip patch array for WLAN frequencies using the circuit and full-wave 3D solvers and optimization tools in CST STUDIO SUITE®. The goal in this case is to design an array with high directivity, low cost and low sidelobes, exhibiting a good impedance matching in the frequency range 5.18 – 5.85 GHz. The same approach can also be used to design other types of array by using a different radiator or array layout.

Patch element

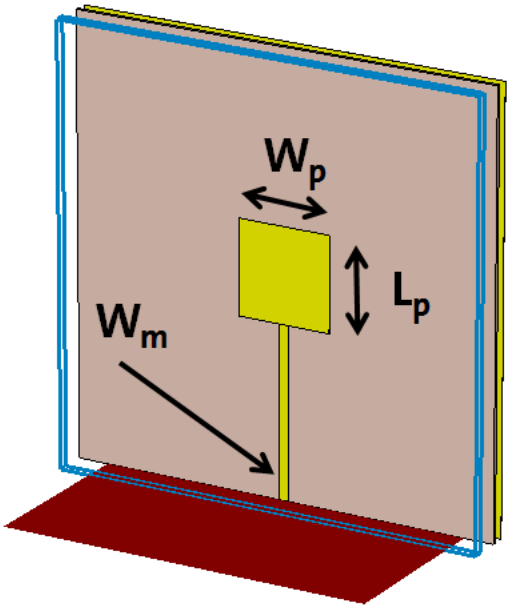

Figure 1: The patch antenna model, showing the variable parameters of the design.

The first step of designing the array is to design the individual element. For this example, a simple square patch antenna was used (Figure 1), and was created directly in CST STUDIO SUITE. The patch is created on a double-layered substrate with an air gap, and is placed inside an ABS box. Two parameters need to be optimized: the length of the patch, in order to adjust the resonant frequency of the patch, and the depth of the air gap, in order to increase its bandwidth.

Array design

Once the individual patch has been designed, it then has to be incorporated into an array. In this case, the choice of box and patch type limits the possible layouts for the array, and so a 4 × 4 planar array is used. However, any arbitrary array shape can be imported as a text file containing the location of each element and the magnitude and phase of the feeding current.

To calculate the gain and directivity of the array, its farfield needs to be found. This can be estimated by multiplying the farfield of the single patch by the array factor, which depends only on the spatial arrangement of the elements and the amplitude and phase of the feeding current of each element. A post-processing tool in CST STUDIO SUITE calculates the array factor and automatically produces a theoretical farfield for an equivalent array. Optimization can then be used to adjust the spacing between the elements to maximize the gain of the antenna, and to change the magnitude of the feeding current to different patches to reduce the side lobes.

Array 3D Simulation

Although the array factor offers a fast, simple way to calculate the farfield for an array, it makes the assumption that the array is ideal, with no coupling or edge effects. A more accurate approach is to simulate the entire array. The Array Wizard in CST STUDIO SUITE will construct an array model from a single element. As shown in Figure 2, the array factor and the full array model are generally in good agreement, even when the ABS casing is included. The largest difference is visible in the backwards radiation pattern. This is due to the larger ground plane and the effect of the edge elements.

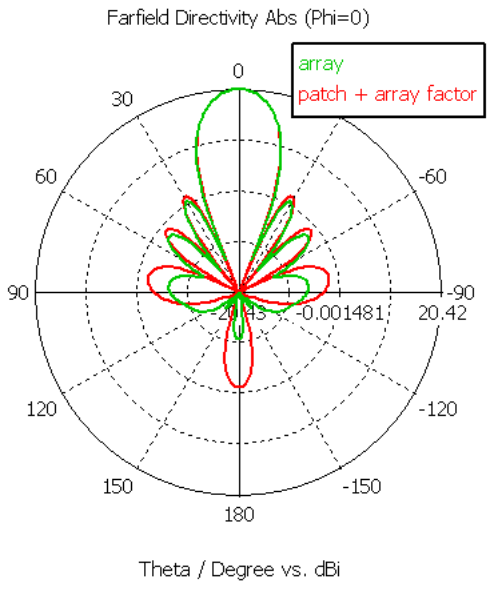

Figure 2: The farfield patterns calculated using the full array model (green) and the array factor method (red), including the effect of the casing.

Feed network

While the individual elements are designed in 3D, the feed network can be created more efficiently using the System Assembly

and Modeling feature of CST STUDIO SUITE. In our case, the patches, ABS box, substrate and aluminum plate are simulated in 3D and the feeding network on a circuit level. Then the complete array will be automatically assembled into 3D in order to investigate the coupling effects in the feeding network.

The array, without the feed network, is automatically assembled and simulated in 3D, with ports defined on each patch. With S-parameter symmetries, only 4 ports need to be excited to calculate the full 16 element S-matrix.

The individual segments of the feed network are treated as multilayer microstrip lines, using the Microstrip Line blocks in the Schematic View (Figure 3). The blocks give an S-parameter representation of the transmission line, and are connected to another block containing the S-parameters from the full-wave simulation of the array without the feed network.

The network is then optimized to maximize the performance of the array. The circuit simulation is very fast, but does not consider 3D effects. Instead, this first optimization gives a good starting point for a more detailed 3D analysis.

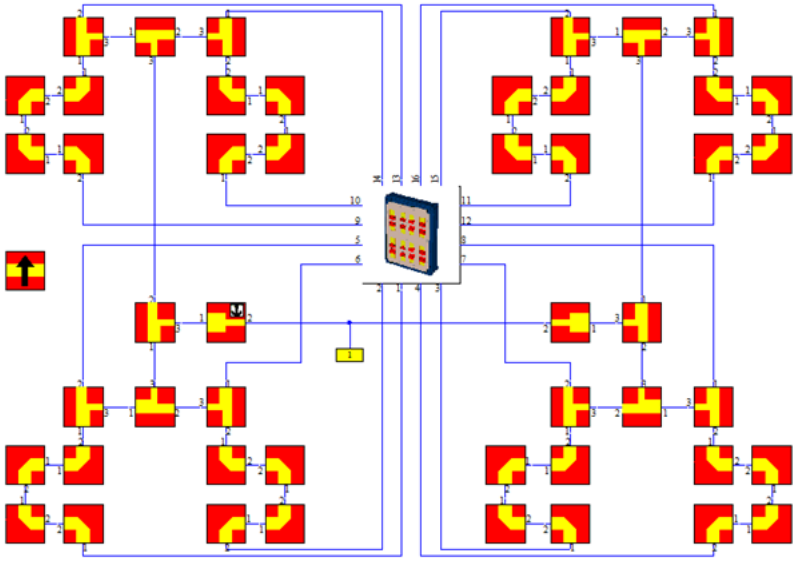

Figure 3: The circuit representation of the feed network. The red circles on the model show the discrete ports.

Feed network 3D simulation

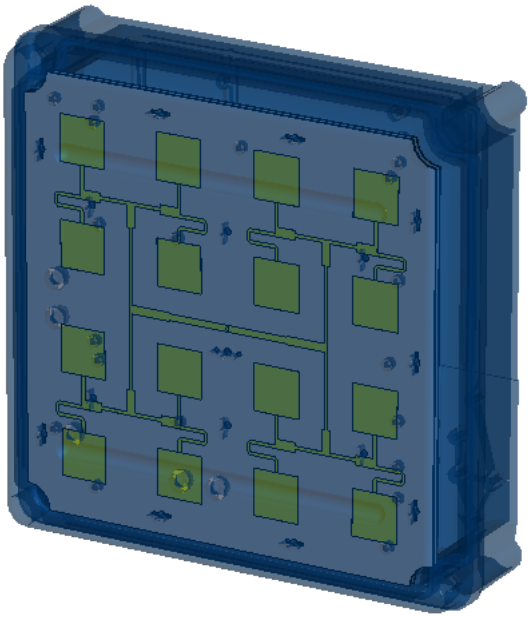

Figure 4: Full 3D model of the array with the feeding network.

The array is again automatically assembled in 3D in the master project (Figure 4). When considered in 3D, the characteristics of the feed network appear slightly different to those calculated using the circuit simulation. This is due to effects such as the coupling between the feed network and the patches, which only appears in a full-wave simulation. These couplings introduce a phase delay, which upsets the excitation of the patches and affect the uniformity of the magnitude distribution.

As a result, a second optimization is used to fine tune the feed network. Since the unwanted interaction between the patches and the feeding lines affects also the radiation pattern, the final optimization should consider both goals on impedance matching and radiation pattern. Because of rather high number of parameters and the complexity the global optimization strategy should be used. GPU computing significantly reduces the optimization time of the whole array. The optimized array satisfied the -15 dB requirements, as shown in Figure 5. The most visible effect of the optimization was to change the length of the meanders so that meanders leading to inner patches are longer than those leading to outer patches. This equalizes the phase difference between the patches and improves the performance of the array. The optimized radiation pattern is depicted in Figure 6.

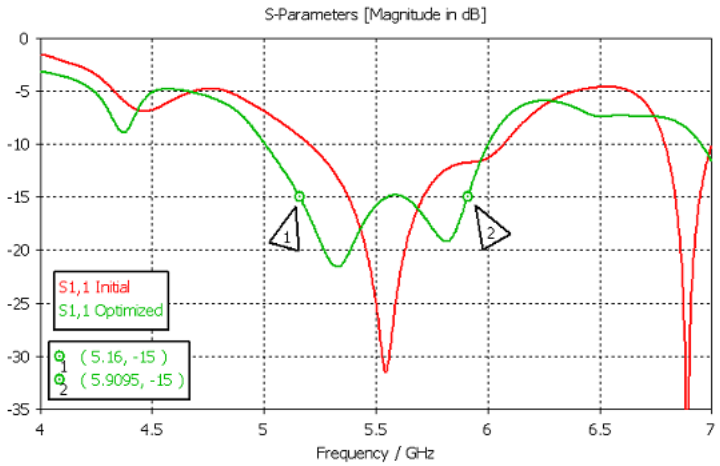

Figure 5: S-parameters of the 3D array model, before (dark red) and after (light green) 3D optimization.

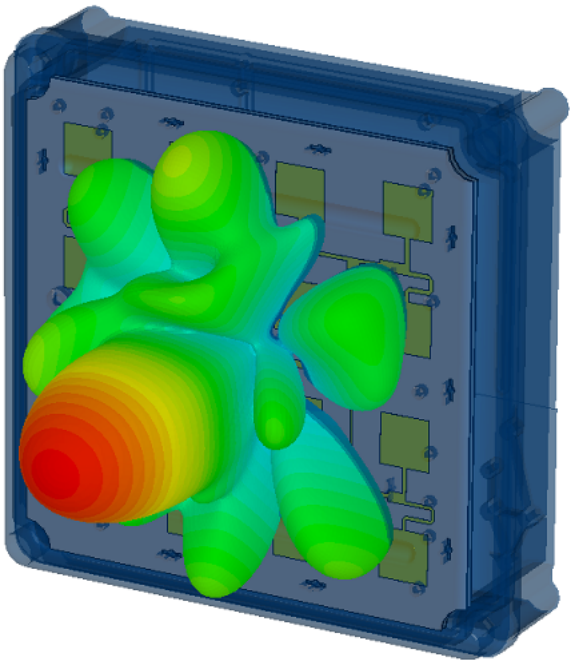

Figure 6: Radiation pattern of the optimized antenna array.

Comparison to measurements

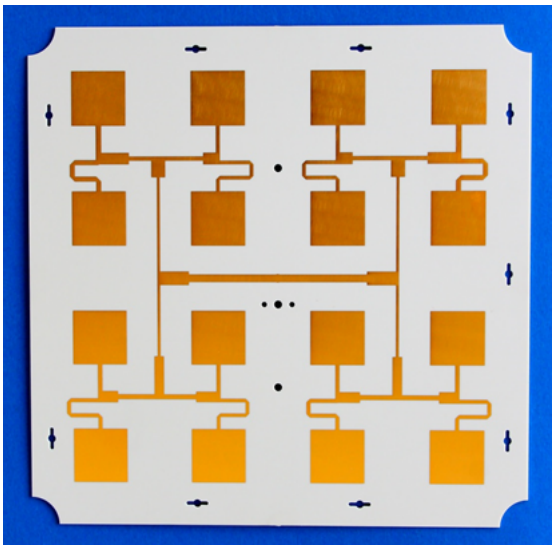

Figure 7: Manufactured PCB with the patch array and integrated feeding network

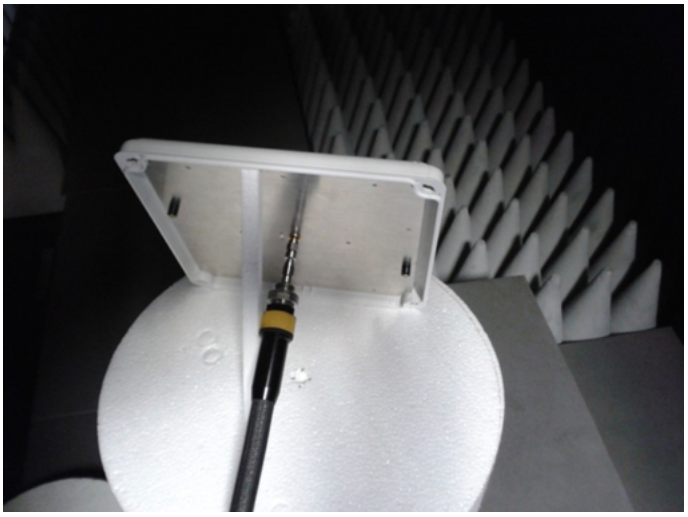

Figure 8: The test set-up in an anechoic chamber, showing the constructed prototype

A prototype of the array (Figures 7 and 8) was constructed and tested in an anechoic chamber, both with and without the ABS front plate. The S-parameter results for the bare array (Figure 9) show a very good agreement between the simulated and measured S-parameters in terms of both magnitude and phase. In this case, the array is sensitive to variations in, for instance, the air gap between the substrate and ground plane, and these are the main source of uncertainity. The difference is slightly greater when the ABS front plate is included (Figure 10) – the front plate introduces additional possible sources for manufacturing variations, and therefore additional uncertainty in the measured results.

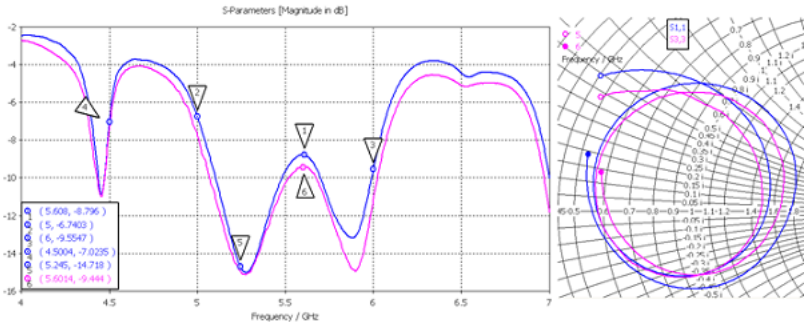

Figure 9: S-parameters for the array without the ABS casing.

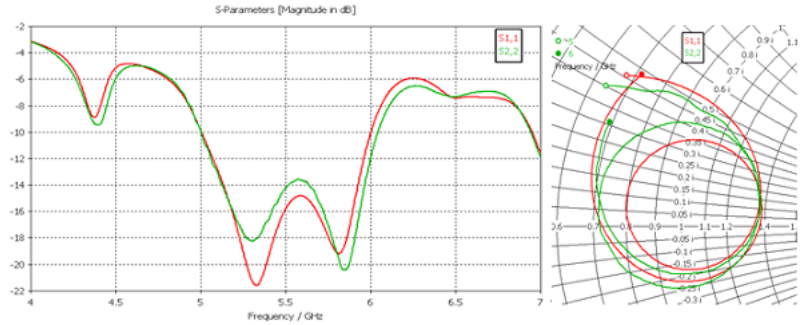

Figure 10: S-parameters for the array with the ABS casing.

The farfield of the array was also measured. Figure 11 shows the gain of the array both as measured and as simulated. The co-polarization results agree very closely, as do the cross-polarization results in the H-plane. The asymmetry in the cross-polarization measurements is due to the metallic fixture, which was not present in the simulation.

The E-plane cross-polarization results do however differ significantly – the theoretical free-space gain of the array, around -140 dB, could not be achieved in the laboratory due to residual reflections in the anechoic chamber and uncertainties in the position of the array. The measured E-plane cross-polarization level of between -10 dBi and -20 dBi is however sufficient considering the much higher H-plane cross-polarization.

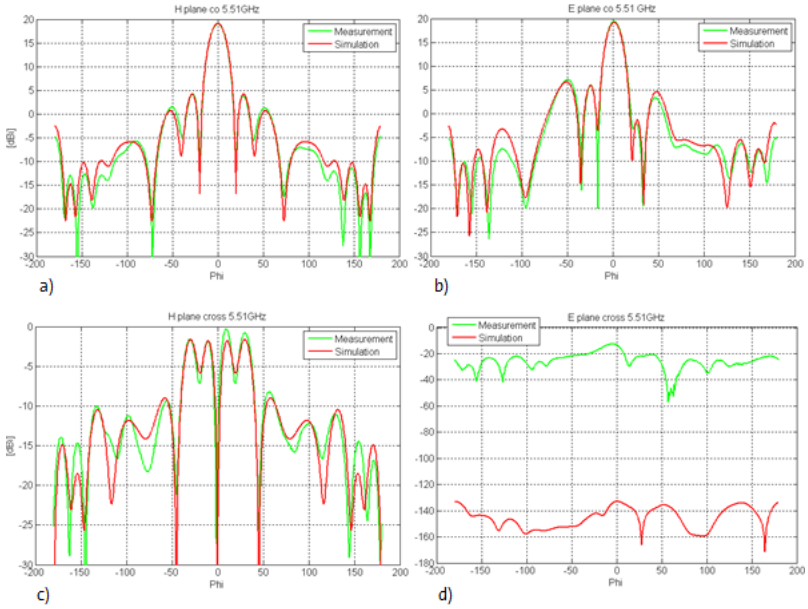

Figure 11: Co-polarization (top) and cross-polarization (bottom) gain in the H-plane (left) and E-plane (right) at 5.51 GHz